WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array formed on the semiconductor substrate, and including a first gate insulator having a first thickness;

a high-voltage transistor circuit formed on the semiconductor substrate, and including a second gate insulator having a second thickness greater than the first thickness; and

a peripheral circuit formed on the semiconductor substrate, and including the second gate insulator.

2. A device according to claim 1, wherein the peripheral circuit is a guard ring, and arranged in a well region formed with the memory cell array.

3. A device according to claim 1, wherein the peripheral circuit is a guard ring, and arranged between the memory cell array and the high-voltage transistor circuit.

4. A device according to claim 3, wherein the guard ring is arranged adjacent to the high-voltage transistor circuit.

5. A device according to claim 1, wherein the peripheral circuit is a dummy pattern, and arranged around the high-voltage transistor circuit.

6. A device according to claim 1, wherein the

high-voltage transistor circuit constitutes a row decoder circuit.

7. A method of manufacturing a non-volatile semiconductor memory device, comprising:

successively depositing a first gate insulator having a first thickness, a first gate electrode film and a first mask insulator on a semiconductor substrate;

leaving the first gate insulator, the first gate electrode film and the first mask insulator in only an array region;

separately forming the following gate insulators in a peripheral region excepting the array region, that is, forming a second gate insulator having a second thickness greater than the first thickness in a first region of a peripheral region, and forming a third gate insulator having a thickness the same as the first thickness in a second region of the peripheral region;

successively depositing a second gate electrode film and a second mask insulator thicker than the first mask insulator on each of the first mask insulator, the second gate insulator and the third gate insulator;

removing the second mask insulator and the second gate electrode film on the first mask insulator;

forming an isolation trench on a surface of the semiconductor substrate to correspond to each position between the array region and first and second regions

of the peripheral region;

depositing a buried insulator on the entire surface; and

polishing an upper surface of the buried insulator so that the upper surface can be planarized.

8. A method according to claim 7, wherein chemical mechanical polishing (CMP) is used to planarize the buried insulator.

9. A method according to claim 7, wherein the first region is formed with a row decoder circuit including a high-voltage transistor, and the second region is formed with a peripheral circuit including a guard ring and a dummy pattern.

10. A method of manufacturing a non-volatile semiconductor memory device, comprising:

successively depositing a first gate insulator having a first thickness, a first gate electrode film and a first mask insulator on a semiconductor substrate;

leaving the first gate insulator, the first gate electrode film and the first mask insulator in only an array region and a first peripheral region;

forming a second gate insulator having a second thickness greater than the first thickness in a second peripheral region excepting the array region and the first peripheral region;

successively depositing a second gate electrode

film thinner than the first gate electrode film and a second mask insulator on each of the first mask insulator and the second gate insulator;

removing the second mask insulator and the second gate electrode film on the first mask insulator;

forming an isolation trench on a surface of the semiconductor substrate to correspond to each position between the array region and first and second regions of the peripheral region;

depositing a buried insulator on the entire surface; and

polishing an upper surface of the buried insulator so that the upper surface can be planarized.

11. A method according to claim 10, wherein chemical mechanical polishing (CMP) is used to planarize the buried insulator.

12. A method according to claim 10, wherein the second mask insulator is formed to have approximately the same height as the first mask insulator.

13. A method according to claim 10, wherein the second peripheral region is formed with a row decoder circuit including a high-voltage transistor circuit.

14. A method according to claim 10, wherein the first peripheral region is formed with a peripheral circuit including a guard ring and a dummy pattern.

15. A method of manufacturing a non-volatile semiconductor memory device, comprising:

previously forming a recess in a first peripheral region on a semiconductor substrate;

forming a first gate insulator having a first thickness in the recess;

forming a second gate insulator having a second thickness less than the first thickness in an array region and a second peripheral region on the semiconductor substrate;

successively depositing first and second gate electrode films and first and second mask insulators on each of the first and second gate insulators;

forming an isolation trench on a surface of the semiconductor substrate to correspond to each position between the array region and the first and second regions of the peripheral region;

depositing a buried insulator on the entire surface; and

polishing an upper surface of the buried insulator so that the upper surface can be planarized.

16. A method according to claim 15, wherein the depth of the recess is substantially the same as the thickness of the first gate insulator.

17. A method according to claim 15, wherein the first and second gate electrode films and the first and second mask insulators are formed to have substantially the same thickness, respectively.

18. A method according to claim 15, wherein the

first peripheral region is formed with a row decoder circuit including a high-voltage transistor circuit.

19. A method according to claim 15, wherein the second peripheral region is formed with a peripheral circuit including a guard ring and a dummy pattern.

20. A method according to claim 15, wherein chemical mechanical polishing (CMP) is used to planarize the buried insulator.